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NASA TECH BRIEF

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Digital Second-Order Phase-Locked Loop

The problem:

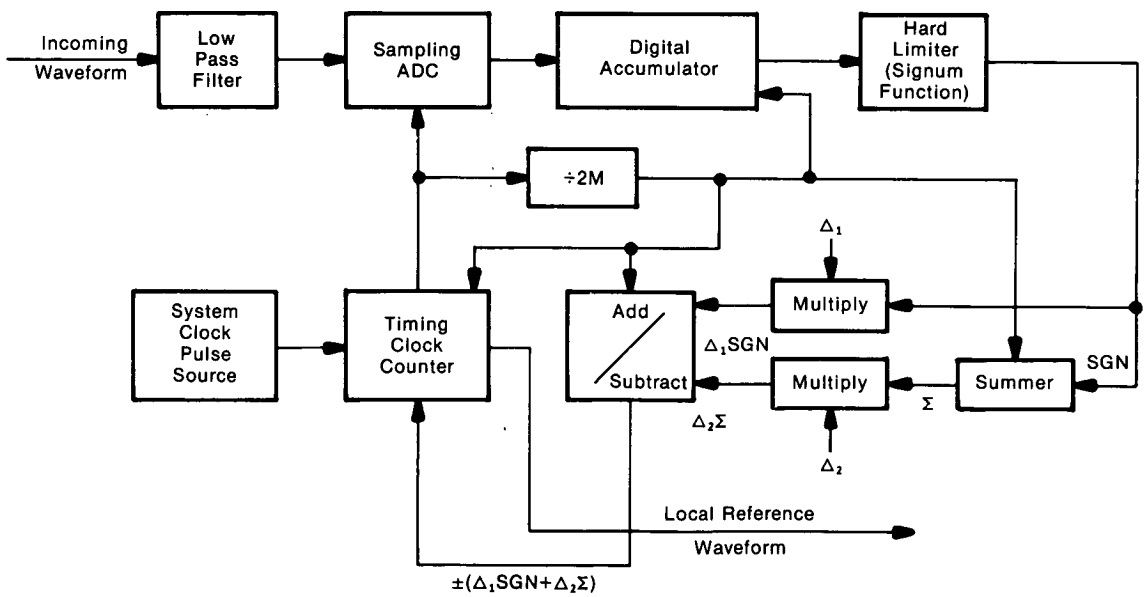
The relative Doppler shift of a telemetry subcarrier, previously thought to be $1x10^{-5}$, was found to be $1x10^{-4}$ in some instances. The Doppler shift of the subcarrier induces a phase error bias in the receiver subcarrier timing that increases with increasing Doppler shift. Because of these facts, a first-order digital phase-locked loop (DPLL) is not adequate for tracking the signal without an appreciable timing error and, in fact, will not lock at a relative frequency offset of $2x10^{-4}$.

The solution:

Actual tests with a second-order DPLL at a simulated relative Doppler shift of $1x10^{-4}$ produced phase lock with a timing error of 6.5° and no appreciable Doppler bias. Thus the loop appears to achieve subcarrier synchronization and to remove the bias due to Doppler shift in the range of interest.

How it's done:

Based on the fact that an analog second-order phase-locked loop (PLL) has no static phase error in



Block Diagram of Second-Order Digital Phase-Locked Loop

(continued overleaf)

the presence of Doppler shift, a linear, analog, PLL model, equivalent to a second-order digital PLL was analyzed and constructed as shown in the block diagram. The loop operates in the same manner as a first-order DPLL except for the addition of the summer branch of the loop filter. The incoming waveform is assumed to be composed of a squarewave subcarrier of amplitude A, with period T_{SC}, and white Gaussian noise of two-sided spectral density $N_0/2$. The low-pass filter cuts off at a frequency of W Hz. The sampler obtains a sufficient number (16) of equally spaced samples per subcarrier cycle to represent the signal adequately.

These samples are then converted to digital format (a four-bit word in this case) by the analog-to-digital converter (ADC). The ADC (which can be thought of as a phase detector) also selects a sample corresponding to the nominal center of the subcarrier transition (zero crossing) every subcarrier period. After accumulating M of these transition samples in the digital accumulator, the accumulation is passed to the hard limiter, which implements the signum (SGN) function. The output of the hard limiter, SGN, which is either +1 or -1, is multiplied by Δ_1 fractions of a subcarrier cycle (FSCC) and then increments the clock timing by $2\pi\Delta_1$ radians. Simultaneously, the sign of the accumulation is added to the summer of the loop filter, and an output equal to Δ_2FSCC, times the value of the summer, increments the clock or transition sampler timing by $2\pi\Delta_2$ radians.

The number M largely determines the bandwidth of the loop and is here chosen for convenience to be equal to the number of subcarrier waveform cycles per data bit period. The values of Δ_1 and Δ_2 are each equal to some number of fractions of a subcarrier cycle and may each be selected as required, the only constraint being that $\Delta_1 > \Delta_2$.

In summary then the loop operates as follows: The phase detector ADC/accumulator produces an output every M subcarrier cycles which is then fed to the filter. The filter in turn controls the time phase of the sampler vis the clock so that the timing is updated by $(\Delta_1 SGN + \Delta_2 \Sigma)$ times 2π radians every M subcarrier cycles.

Note:

Requests for further information may be directed to:

Technology Utilization Officer
NASA Pasadena Office
4800 Oak Grove Drive
Pasadena, California 91103
Reference: TSP74-10274

Patent status:

This invention has been patented by NASA (U.S. Patent No. 3,777,272). Inquiries concerning nonexclusive or exclusive license for its commercial development should be addressed to:

Patent Counsel
NASA Pasadena Office
4800 Oak Grove Drive
Pasadena, California 91103

Source: Jack K. Holmes,
Christopher Carl, and
Carl R. Tagnelia of
Caltech/JPL
under contract to
NASA Pasadena Office
(NPO-11905)

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